What is claimed is:

1. A processor comprising

private memory; and

one or more execution units to authenticate an authenticated code module stored in the private memory and to execute the authenticated code module stored in the private memory in response to executing a launch instruction.

2. The processor of claim 1 further comprising a cache memory that provides the private memory.

3. The processor of claim 2 wherein the execution units load authentication code module into the cache memory in response to executing the launch instruction.

4. The processor of claim 3 wherein the execution units lock the cache memory to prevent replacement of lines of the authenticated code module stored in the cache memory.

5. The processor of claim 1 wherein the execution units lock the private memory to prevent other processors from altering the authenticated code module stored in the private memory.

6. The processor of claim 1 further comprising a decoder to generate one or more opcodes for the launch instruction, wherein the execution units authenticate and

execute the authenticated code module in response to executing the one or more opcodes.

7. The processor of claim 1 further comprising a key, wherein the execution units utilize the key to authenticate the authenticated code module.

8. The processor of claim 1, wherein the execution units retrieve a key specified by one or more operands of the launch instruction and use the key to authenticate the authenticated code module stored in the protected memory.

9. The processor of claim 1, wherein the execution units, in response to the launch instruction, retrieve a key from a chipset and use the key to authenticate the authenticated code module stored in the protected memory.

10. The processor of claim 1, wherein the execution units, in response to the launch instruction, retrieve a key from a token and use the key to authenticate the authenticated code module stored in the protected memory.

11. The processor of claim 1, wherein the execution units, in response to the launch instruction, use a key of the processor to authenticate the authenticated code module stored in the protected memory.

12. The processor of claim 1, wherein the execution units, in response to the launch instruction, decrypt at least a portion of the authentication module stored in the private memory.

13. The processor of claim 1, wherein the execution units, in response to the launch instruction, decrypt at least a portion of the authentication module to obtain a digest value, and determine whether the authentication module is authentic based upon the digest value.

14. The processor of claim 1, wherein the execution units, in response to the launch instruction, obtain a digest value for the authentication code module, generate a computed digest value from at least a portion of the authenticated code module, and determine that the authenticated code module is authentic in response to the digest value and the computed digest value having a predetermined relationship.

15. The processor of claim 1, wherein the execution units, in response to the launch instruction, RSA-decrypt a signature of the authentication code module to obtain a digest value from the signature, perform a SHA-1 hash on the authenticated code module to generate a computed digest value, and determine that the authenticated code module is authentic in response to the digest value and the computed digest value being equal.

16. The processor of claim 1, wherein the execution units initiate execution of the authenticated code module only if the authenticated code module is determined to be authentic.

17. The processor of claim 16, wherein the execution units generate an error code in response to determining that the authenticated code module is not authentic.

18. The processor of claim 17, wherein the execution units generate a trap in response to determining that the authenticated code module is not authentic.

19. The processor of claim 1, wherein the execution units execute the authenticated code module from a execution point specified by one or more operands of the launch instruction.

20. The processor of claim 1, wherein the execution units execute the authenticated code module from an execution point specified by one or more fields of the authenticate code module.

21. The processor of claim 1, wherein the execution units mask one or more events selected from a group of events comprising INTR, NMI, SMI, INIT, and A20M events in response to executing the launch instruction.

22. The processor of claim 1, wherein the execution units authenticate and initiate execution of the authenticated code module stored in the private memory in response to executing microcode associated with the launch AC instruction.

23. The processor of claim 1, embodied in a machine readable medium.

24. A processor, comprising

a front end to fetch an instruction; and

one or more execution units to execute the instruction that results in the one or more execution units retrieving a key and authenticating an authenticated code module.

25. The processor of claim 24, wherein the front end generates one or more ops for the instruction, and execution of the instruction results in the execution units executing the one or more ops.

26. The processor of claim 24 further comprising a processor key, wherein execution of the instruction results in the execution units authenticating the authenticated code module based upon the processor key.

27. The processor of claim 24, wherein execution of the instruction results in the execution units loading the authenticated code module into a private memory associated with the processor.

28. The processor of claim 24, wherein execution of the instruction results in the execution units obtaining a digest value from the authenticated code module, hashing the authenticated code module to generate a computed digest value, and initiating execution of the authenticated code module in response to the digest value and the computed digest value having a predetermined relationship.

29. The processor of claim 28, wherein execution of the instruction results in the execution units generating an error code in response to determining that the digest value and the computed digest value do not have the predetermined relationship.

30. The processor of claim 28, wherein execution of the instruction results in the execution units initiating execution of the authenticated code module from an execution point specified by one or more operands of the instruction.

31. The processor of claim 24, wherein execution of the instruction results in the execution units initiating execution of the authenticated code module from an execution point specified by one or more fields of the authenticate code module.

32. The processor of claim 24, wherein the execution units authenticate the authenticated code module in response to executing microcode of the processor.

33. The processor of claim 24, embodied in a machine readable medium.

34. A processor, comprising

a cache memory;

a front end to fetch an instruction; and

one or more execution units to execute the instruction that results in the one or more execution units loading an authentication module into the cache memory and authenticating the authenticated code module stored in the cache memory.

35. The processor of claim 34, wherein the execution units initiate execution of the authenticated code module stored in the cache memory in response to determining that the authenticated code module is authentic.

36. The processor of claim 35, wherein the execution units retrieve a key and authenticate the authenticated code module based upon the key.

37. The processor of claim 36, wherein the execution units obtain a digest value by decrypting a portion of the authenticated code module with the key, generated a computed digest value, and determine authenticity of the authenticated code based upon a relationship between the digest value and the computed digest value.

38. The processor of claim 36, wherein the execution units retrieve the key and authenticate the authenticated code module in response to executing microcode.

39. The processor of claim 38 embodied in a machine readable medium.